IN THE SPECIFICATION:

Please amend paragraph **[0020]** as follows:

[0020] ~~Figure~~ FIG. 1 is a cross-sectional view of a planarized insulation layer having therein a contact hole, the insulation layer being situated on a semiconductor substrate, and a metallization layer being disposed upon the insulation layer over the contact hole that is not filled by the metallization layer.

Please amend paragraph **[0021]** as follows:

[0021] ~~Figure~~ FIG. 2 is a cross-sectional view of the structure seen in ~~Figure~~ FIG. 1, where the metallization layer fills the contact hole, and the metallization layer has a non-planar top surface above the insulation layer

Please amend paragraph **[0022]** as follows:

[0022] ~~Figure~~ FIG. 3 is a cross-sectional view of the structure seen in ~~Figure~~ FIG. 2, where the metallization layer is planarized at the top surface of the insulation layer so as to isolate within the insulation layer a plug in the contact hole.

Please amend paragraph **[0023]** as follows:

[0023] ~~Figure~~ FIG. 4 is a cross-sectional view of the structure seen in ~~Figure~~ FIG. 3, where a second metallization layer is formed over the insulation layer on and above the isolated plug in the contact hole, and also showing in a graphic form an optional thermal diffusion of a preferred alloying element from the second metallization layer into the first metallization layer in the contact hole.

Please amend paragraph **[0024]** as follows:

[0024] ~~Figure~~ FIG. 5 is a cross-sectional view of the structure seen in ~~Figure~~ FIG. 3, and further illustrates a partial etch of the insulation layer below the extent of the plug and thereby exposing lateral surfaces below the top surface thereof, followed by the formation of a

second metal layer over the insulation layer and over the top and exposed lateral surfaces of the plug, the top surface of the second metal layer having been planarized to a preferred thickness suitable for metallization lines.

Please amend paragraph **[0025]** as follows:

[0025] ~~Figure~~ FIG. 6 is a cross-sectional view of a planarized insulation layer having therein a contact hole, the insulation layer being situated on a semiconductor substrate, and a metallization layer being disposed upon the insulation layer over the contact hole filled by the metallization layer, the metallization layer having been planarized above the insulation layer to a preferred thickness suitable for metallization lines.

Please amend paragraph **[0026]** as follows:

[0026] ~~Figure~~ FIG. 7 is a cross-sectional view of the structure seen in ~~Figure~~ FIG. 3, and further illustrates a refractory metal silicide layer at the bottom of the contact hole, the contact hole being lined by a refractory metal nitride layer, the plug being in contact with both the refractory metal silicide layer and the refractory metal nitride layer, and a second metal layer over the insulation layer and over the top of the plug, the refractory metal silicide layer, and the refractory metal nitride layer, the top surface of the second metal layer having been planarized to a preferred thickness suitable for metallization lines.

Please amend paragraph **[0027]** as follows:

[0027] ~~Figure~~ FIG. 8 is a section taken along the line 8--8 from ~~Figure~~ FIG. 7 in which the contact plug has a second end opposite the first end in contact with the refractory metal silicide layer at the bottom of the contact hole; the second end is in contact with a second refractory metal silicide layer, the second refractory metal silicide layer being in contact with the metallization line.

Please amend paragraph **[0031]** as follows:

[0031] Because aluminum has a melting point of about ~~660°C~~ 660° C, substantially lower than that of tungsten (~~3,370°C~~ 3,370° C) or titanium (~~1,800°C~~ 1,800° C), achieving ductility sufficient to cause pressure or reflow filling of the contact hole comes at significantly lower temperatures for aluminum. For example, aluminum alone has a melting point that is about 26 percent of the melting point of tungsten, about 37 percent of the melting point of copper, and about 46 percent of the melting point of silicon. Adding preferred amounts of copper- and/or silicon-alloying elements does not significantly cause the pressure fill or reflow temperatures to materially approach those required of a titanium plug fill in the contact hole (about 57 percent of tungsten) or of tungsten plug fill in the contact hole.

Please amend paragraph **[0032]** as follows:

[0032] ~~Figure~~ FIG. 1 illustrates the first step in the inventive method in which a semiconductor device 10 has an insulation layer 14 disposed upon a semi-conductive device substrate 12. A contact hole 16 has been formed, such as by patterning and etching, within insulation layer 14. Contact hole 16 exposes semiconductor substrate 12 and a first metallization layer 18 has been formed, such as by deposition, upon insulation layer 14.

Please amend paragraph **[0034]** as follows:

[0034] ~~Figure~~ FIG. 2 illustrates the result of a pressure filling step in filling contact hole 16 with first metallization layer 18. A topographical depression forms in first metallization layer 18 above contact hole 16, caused by the filling of first metallization layer 18 into contact hole 16. Removal of at least some of first metallization layer 18 is next required to planarize the same. After formation of first metallization layer 18, an optional heat treatment is carried out to anneal structures of semiconductor device 10.

Please amend paragraph **[0035]** as follows:

[0035] ~~Figure~~ FIG. 3 illustrates the result of a planarization step that stops on insulation layer 14. The planarizing step can be either a mechanical planarizing step of a chemical mechanical planarization step (CMP). After the planarization step, only a contact plug 19 remains of first metallization layer 18. Contact plug 19, which is isolated by insulation layer 14, fills contact hole 16. A mechanical planarization step is costly in both time and materials. Mechanical planarization also requires a cleaning step before the wafer can be advanced to the next process step. If a chemical mechanical planarization process (CMP) is used to planarize and then stop on insulation layer 14, as shown in ~~Figure~~ FIG. 3, chemicals in the CMP process oxidize upper surfaces of first metallization layer 18 and abrasives therein shear away oxides of the upper surfaces of first metallization layer 18 in a repeating cycle that eventually planarizes first metallization layer 18.

Please amend paragraph **[0036]** as follows:

[0036] Following planarization, a second metallization layer 20 seen in ~~Figure~~ FIG. 4 is formed upon insulation layer 14. Second metallization layer 20, like first metallization layer 18, can be formed by PVD, CVD, or variations thereof. Second metallization layer 20 is formed upon an exposed end of isolated contact plug 19. A second planarization step is carried out to planarize the exposed upper surface of second metallization layer 20. This second planarization step is performed until second metallization layer 20 has a preferred metallization line thickness. Like the first planarization step, the second planarization step can be either a mechanical planarization step or a chemical mechanical planarization step.

Please amend paragraph **[0039]** as follows:

[0039] Another method of the present invention, illustrated in ~~Figure~~ FIG. 6, involves forming sole metallization layer 22 upon insulation layer 14. If sole metallization layer 22 does not fill contact hole 16 when it is formed, procedures for filling contact hole 16 are implemented as described above. Planarization of sole metallization layer 22, such as by a mechanical or

chemical-mechanical planarization process, is then undertaken. Planarization of sole metallization layer 22, however, does not expose insulation layer 14, but rather achieves a desired thickness upon insulation layer 14. Planarized sole metallization layer 22 and contact plug 19 are an integral structure, thus providing for one less metal-to-metal interface when compared with the structure seen in ~~Figures~~ FIGs. 4 and 5. Few metal-to-metal interfaces will correspondingly reduce resistance to current flow, in that a metal-to-metal interface may have discontinuities that cause resistance at the interface to be higher, which in turn causes the inherent inefficiency of Joule heating to occur.

Please amend paragraph **[0040]** as follows:

[0040] Another method of the present invention involves diffusive heat treating of isolated contact plug and second metallization layer 20. The procedures as set forth above for ~~Figures~~ FIGs. 1-5 are followed. For first metallization layer 18, specific alloys are selected that allow for substantially complete filling of contact hole 16. In the case of second metallization layer 20, specific alloys are selected that allow for an excess of a preferred alloying element to be present. After the selection and use of the selected specific alloys in first and second metallization layers 18, 20, a heat treatment step is carried out following the formation of second metallization layer 20. The heat treatment is conducted for a time period sufficient to allow a selected amount of a preferred alloying element to diffuse from a region of higher concentration within second metallization layer 20 to a region of lower concentration in isolated contact plug 19.

Please amend paragraph **[0042]** as follows:

[0042] ~~Figure~~ FIG. 4 illustrates, in the graph seen therein, one result of the diffusion methods set forth above. The result of the heat treatment and its induced diffusion is that a substantially uniform concentration gradient of the preferred alloying element is exhibited at an interface B between isolated contact plug 19 and second metallization layer 20. The graph in ~~Figure~~ FIG. 4 illustrates this substantially uniform concentration gradient of a preferred alloying

element taken along the line A--A and including interface B. The graph depicts distance (X) from semiconductor substrate 12 toward second metallization layer 20 with respect to concentration (Y) of a preferred alloying element. In this embodiment, diffusion is illustrated as having proceeded from second metallization layer 20 into isolated contact plug 19. Diffusion, however, can also proceed from isolated contact plug 19 into second metallization layer 20.

Please amend paragraph **[0044]** as follows:

[0044] Another quality is resistance to metal creep that is normally caused by physically interfaced metals of disparate thermal expansion coefficients. By causing a substantially uniform concentration gradient of a preferred alloying element between isolated contact plug 19 and second metallization layer 20, the tendency for metal creep is lessened as the composition at interface B, seen in ~~Figure~~ FIG. 4, can be substantially the same on both sides of interface B. Alternatively the composition on either side of interface B can be of two different types but with substantially equivalent coefficients of thermal expansion at B.

Please amend paragraph **[0045]** as follows:

[0045] Another quality achieved in methods of the present invention is the avoidance of creating large and irregular grain structures in the metallization. These problematic grain structures are avoided when lower processing temperatures, such as those required for aluminum or a lightly doped aluminum alloy, are used to fill contact hole 16. Because aluminum has a melting point of about ~~660°C~~ 660° C, substantially lower than that of tungsten (~~3,370°C~~3,370° C) or titanium (~~1,800°C~~1,800° C), achieving ductility sufficient to cause pressure or reflow contact hole filling comes at significantly lower temperatures. For example, aluminum alone has a melting point that is about 26 percent that of tungsten, copper, about 37 percent, and silicon, about 46 percent. Adding preferred amounts of copper and/or silicon alloying elements does not significantly cause the pressure fill or reflow temperatures to materially approach those required of a titanium plug fill (about 57 percent of tungsten) or of a tungsten plug fill.

Please amend paragraph **[0047]** as follows:

[0047] Another method of the present invention is illustrated in ~~Figure~~ FIG. 6. This method involves etching first metallization layer 18 to expose insulation layer 14, and then exposing lateral surfaces 24 of isolated contact plug 19. This method can be carried out by a single planarizing step, such as mechanical or chemical mechanical planarization, that will remove insulation layer 14 faster than first metallization layer 18 is removed, with some of each being removed by the planarizing step. When a chemical mechanical planarization step is used, the chemistry thereof requires that physically shearable surfaces are created in both first metallization layer 18 and in insulation layer 14, but that between these two, the etch is more selective to first metallization layer 18 than insulation layer 14. An alternative to achieve the same structure with exposed lateral surfaces 24 is to stop on insulation layer 14 in a CMP step and conduct a second etch that is selective to isolated contact plug 19.

Please amend paragraph **[0048]** as follows:

[0048] The methods illustrated in ~~Figures~~ FIGs. 1-7 can be modified by forming a refractory metal nitride lining 26 and a refractory metal silicide ~~layer 24~~ layer 30 at an interface between contact plug 19 and semiconductor substrate 12. This modification allows the use of materials other than aluminum for forming contact plug 19. In one embodiment, a tungsten plug is formed. In so doing, a refractory metal nitride is deposited in contact hole 16 lining the sides of contact hole 16. The refractory metal nitride is then annealed. In the case where semiconductor substrate 12 comprises a silicon substrate, a refractory metal silicide layer 30 is formed at the bottom of contact hole 16 upon semiconductor substrate 12. The anneal also improves the barrier properties of the refractory metal nitride, which prevents diffusion and chemical attack of the chemistry used to deposit the tungsten or other conductive material. Tungsten is then deposited to form contact plug 19. The steps of depositing first metallization layer 18 follow with variations as proposed above with respect to ~~Figures~~ FIGs. 1-8.

Please amend paragraph **[0049]** as follows:

[0049] The present invention also includes a contact plug and metallization line structure according to ~~Figures~~ FIGs. 7 and 8. The contact plug and metallization line structure includes semiconductor substrate 12 having a contact surface thereon. It also includes insulation layer 14 having contact hole 16 therethrough extending to the contact surface of semiconductor substrate 12. Additionally, it includes contact plug 19 substantially composed of a first metal and situated in contact hole 16, contact plug 19 being electrically insulated by insulation layer 14. Second metallization layer 20 is substantially composed of a second metal, wherein contact plug 19 and second metallization layer 20 are electrically connected and have a substantially continuous composition gradient of a selected alloying element between the first metal and the second metal. The contact surface of semiconductor substrate 12 has first refractory metal silicide layer 30 thereon in contact with a first end of the plug 19. Contact hole 16 has an inside wall upon which a refractory metal nitride layer is situated in contact with the insulation layer and the plug. Additionally, contact plug 19 has a second end opposite the first end and in contact with a second refractory metal silicide layer 34 as seen in ~~Figure~~ FIG. 8. Second refractory metal silicide layer 34 is in contact with second metallization layer 20.